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ANALYTICAL INVESTIGATION OF NEUTRON HARDENING OF INTEGRATED INJECTION LOGIC

LEVEL II

Mission Research Corporation
1400 San Mateo Blvd. SE, Suite A
Albuquerque, New Mexico 87108

11 July 1980

Final Report for Period 28 January 1980—11 July 1980

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20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

An analytical technique is presented for investigating the neutron induced degradation of integrated injection logic (I^2L) inverter cells as a function of basic processing variables. The technique combines a one-dimensional semiconductor device code, the PN code, with the circuit analysis code SPICE. Predictions of neutron induced degradation as a function of npn transistor base doping, epitaxial thickness and resistivity and pnp transistor base width are presented for a second generation I^2L technology.

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20. ABSTRACT (Continued)

A comparison of predicted response to experimental data is given for inverter cells fabricated with different npn base doping and epitaxial thickness.

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INTRODUCTION

Modeling the neutron degradation of I^2L inverters has previously been performed[1,2] using specially written computer programs based on closed form expressions for the various cell current components. Component parameter expressions were derived in terms of idealized cell geometry, carrier diffusion coefficients, carrier lifetimes and doping density.

The modeling approach used in this study differs in that the comprehensive one-dimensional device physics PN code is used to obtain the characteristics of the inverter cell elements. The PN code[3] performs a numerical integration of the continuity and Poisson's equations for an arbitrary diffusion profile. Calculated results are then a more exact solution of the I^2L transistor and parasitic diode element characteristics over the whole current range of operation. These characteristics are then used to obtain the SPICE[4] bipolar transistor and diode model parameters for use in a circuit simulation of the I^2L inverter cell[5]. Using this combined approach the terminal response of the inverter cell can be predicted from a knowledge of cell geometry, doping profiles, and carrier lifetimes. The degraded characteristics of the cell elements after neutron irradiation are determined from degraded carrier lifetimes using known lifetime damage coefficients. The degraded performance of the inverter cell is then determined from the degraded component characteristics.

This modeling approach was applied to the second generation I^2L technology at Texas Instruments in order to determine what processing variations could be made to the standard commercial process in order to increase the neutron induced failure levels. This effort is part of a Defense Nuclear Agency program to increase the overall radiation hardness of bipolar LSI technologies.

PN CODE PREDICTIONS

The PN code is used to determine the current versus voltage characteristics of the I^2L inverter components. These components consist of a lateral pnp injector transistor, a vertical npn switching transistor and a vertical parasitic diode. These elements are shown in Figure 1 which consists of a top surface and cross-sectional view of a four output inverter cell representative of the second generation I^2L technology used in this study[6]. The process utilizes a thin n type epitaxial layer on an n+ substrate. A deep heavily doped, p diffusion is used for the injector and extrinsic npn base (also pnp collector). The npn intrinsic base consists of a p^- implant and the npn collector epitaxial region has a shallow n+ contact diffusion. The cells are surrounded by an oxide sidewall to prevent sidewall injection.

The inputs to the PN code consist of the doping profile (input at up to 30 mesh regions), cross-sectional area, a table of mobility versus doping density, carrier lifetimes at up to twenty locations in the profile, energy level of carrier recombination center, avalanche and tunneling parameters (if desired), exterior resistance, capacitance and inductance, and terminal voltages versus time.

The doping profiles for the I^2L elements of the standard commercial process were obtained from the manufacturer. These profiles were determined using the computer code SUPREM which calculates a diffusion and/or implant profile based on processing schedule parameters such as diffusant type and concentration, diffusion times and temperatures and implant energies and fluence. The diffusion and implant depths and epitaxial thickness were verified with angle lap and stain data taken by NWSC Crane. The doping profiles for the standard process npn and pnp transistors are given in Figures 2 and 3 respectively. The npn profile is shown from the top surface down and the pnp profile is taken from the center of the

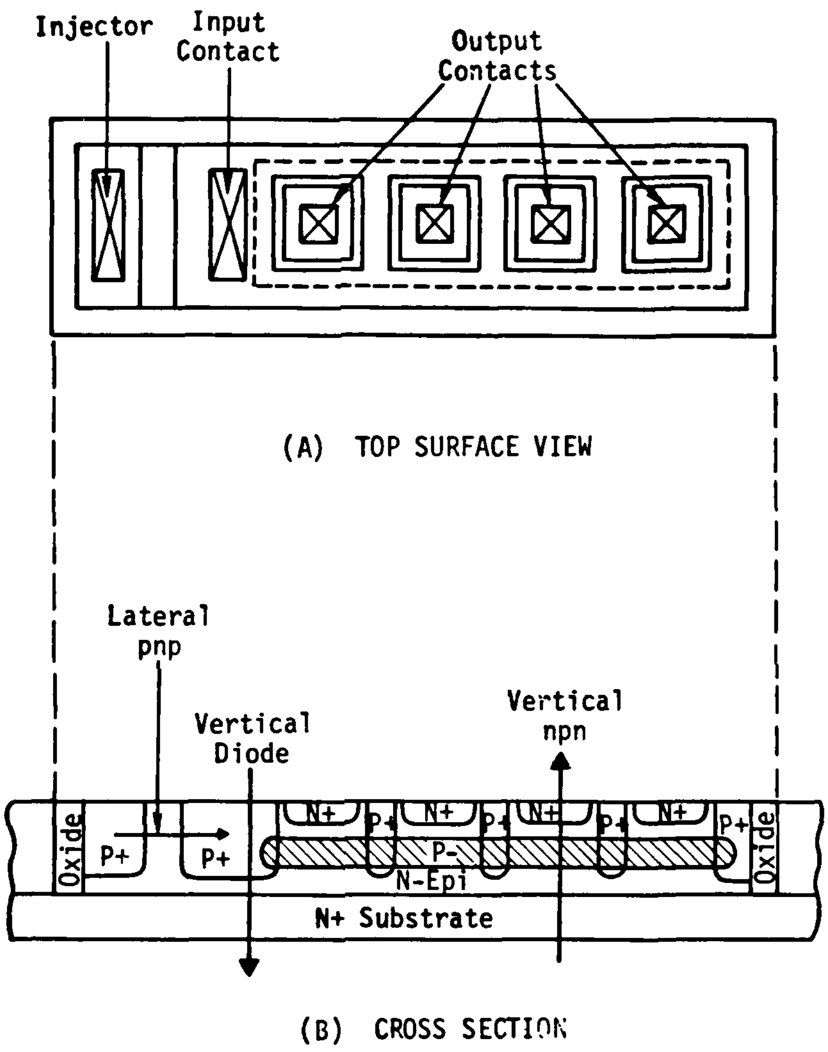

Figure 1. Top surface and cross sectional view of I^2L four output inverter cell used in study.

injector contact to the center of the input contact on a horizontal line half way between the surface and the bottom of the P+ diffusion. The profiles in Figures 2 and 3 are shown point by point as input to the PN code. These points define the mesh regions. The user inputs the number of mesh points within each region and the code performs a linear interpolation between mesh regions to determine the doping density at each mesh point. Up to 300 total mesh points were allowed with the version of the PN code used in this study.

The preirradiation carrier lifetimes were taken from a least squares fit of transistor lifetimes versus doping density using data from published and unpublished reports[7,8]. A plot of this data is given in Figure 4. The energy level for the single level SRH recombination model used in the PN code was taken to be at the center of the silicon band gap.

In order to determine the DC input parameters for the Gummel-Poon (GP) bipolar transistor model used in SPICE, a forward biased base-emitter voltage was applied to the transistor, with $V_{BC} = 0$, and the base and collector currents (I_B, I_C) were determined. The I_B and I_C values, taken in 0.1 V steps from $V_{BE} = 0$ to $V_{BE} = 0.9$ V, were plotted and the GP model parameters determined graphically. In a similar manner, the parasitic diode I-V characteristic was calculated, and the SPICE diode model parameters determined.

SPICE CIRCUIT ANALYSIS

The SPICE circuit analysis code was used to determine the fanout per collector versus the output current for a four output inverter. The circuit representation of the inverter cell[5] is shown in Figure 5. The fanout per collector is determined by applying a voltage to the input terminal with the injector grounded and measuring the ratio of output current to input current as was done experimentally.

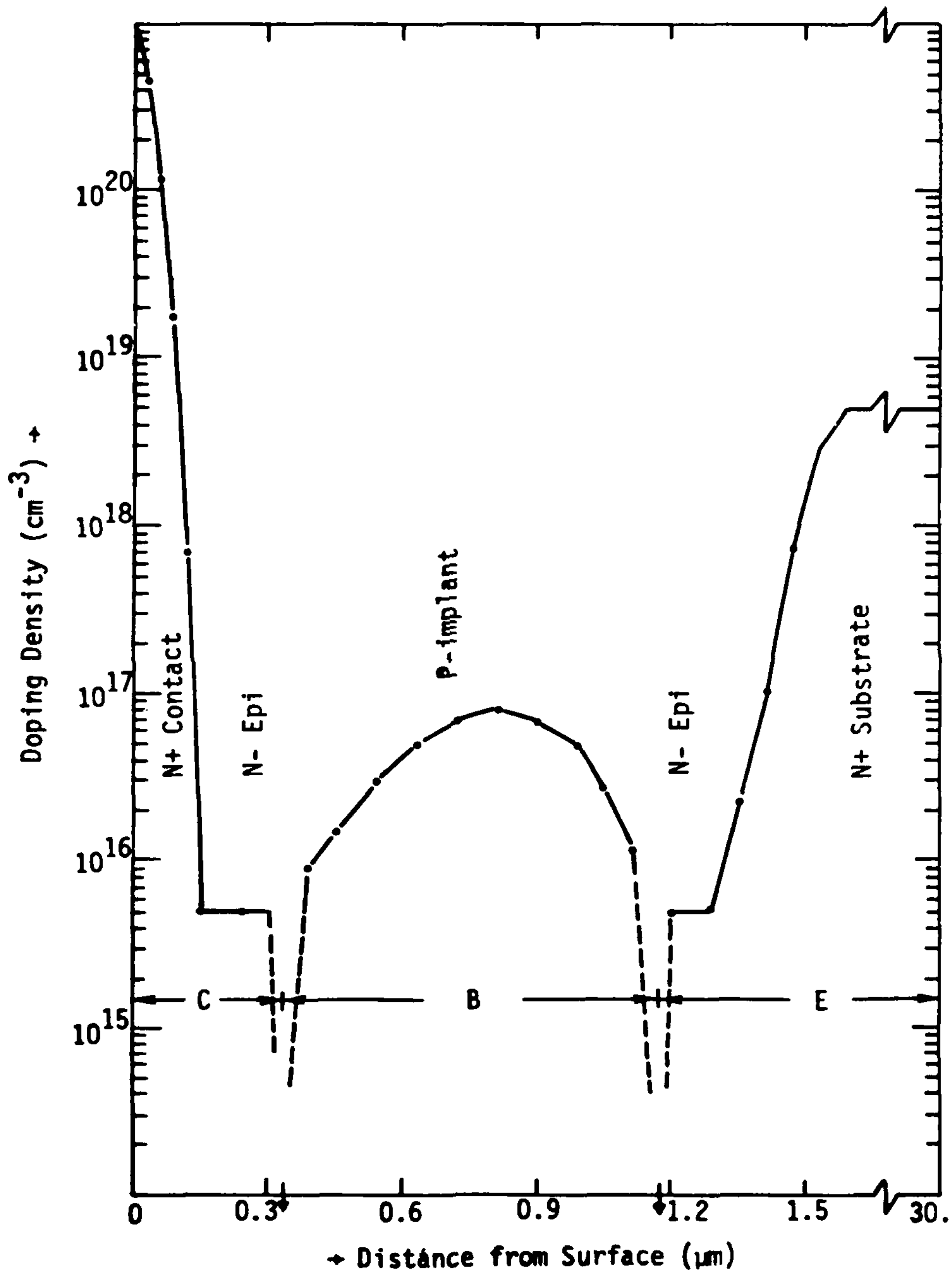

Figure 2. Verticle NPN transistor doping profile used for standard process. (Taken from SUPREM calculation.)

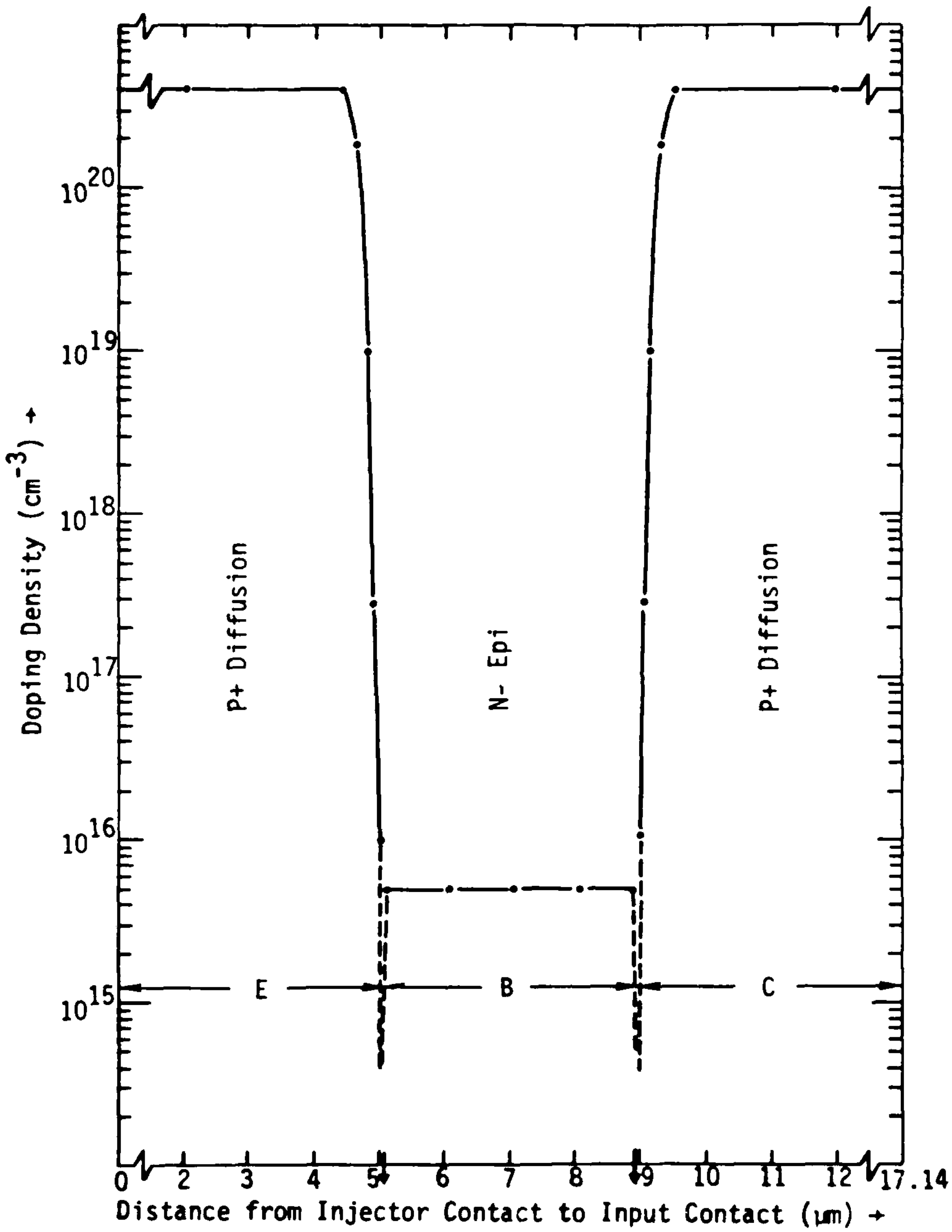

Figure 3. Horizontal PNP transistor doping profile used for standard process. (Taken from SUPREM calculation.)

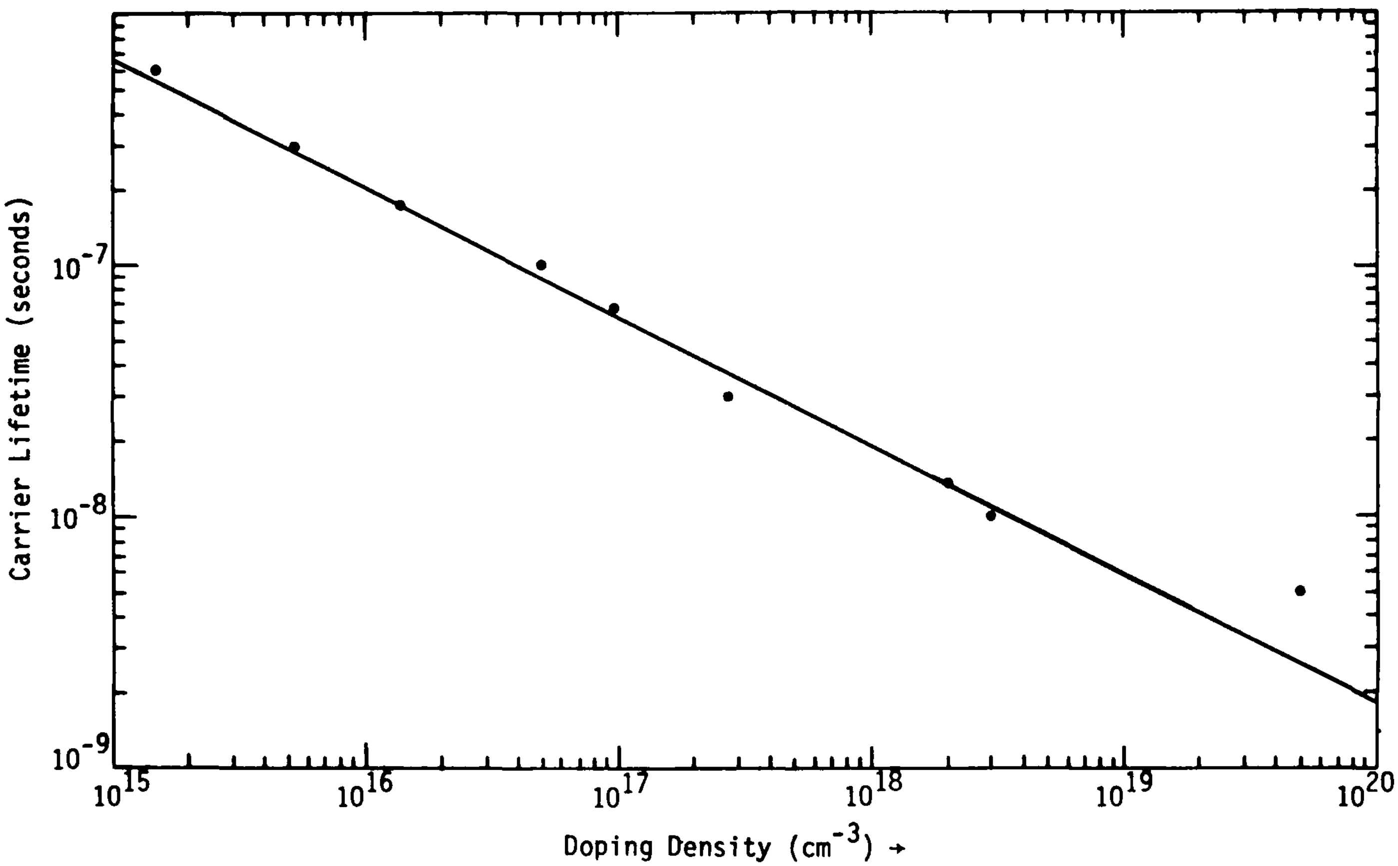

Figure 4. Transistor minority carrier lifetime versus doping density.

$$\text{Fanout} = \frac{\text{Output Current}}{\text{Input Current}} \quad (V_{INJ} = 0)$$

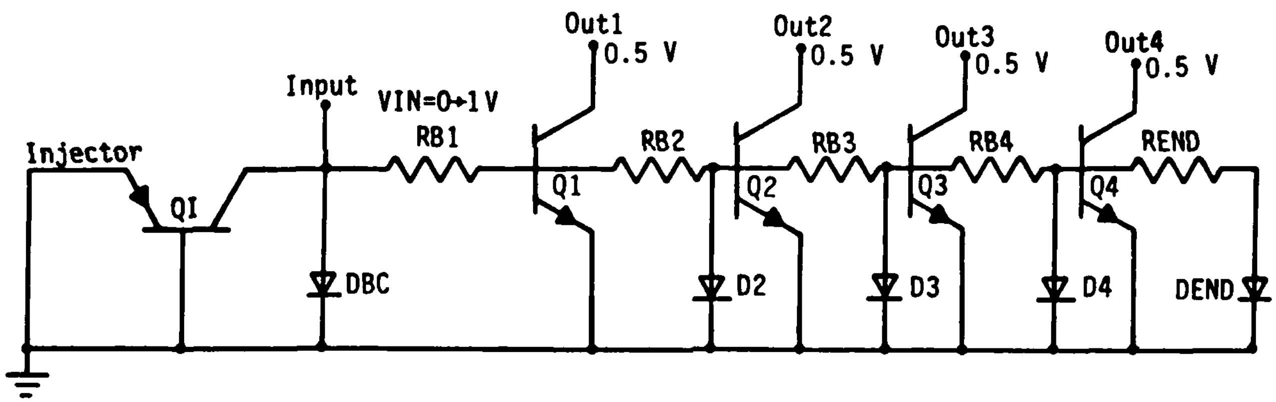

Figure 5. Circuit representation of 4 output inverter cell used to determine fanout.

The resistance RB1 is the extrinsic base resistance from the input contact to the first collector. RB2, 3 and 4 are extrinsic base resistances between collectors and REND is the resistance of the base end section. These resistances were calculated from a knowledge of the cell geometry and the sheet ρ of the P^+ diffusion. The parasitic diode, DBC, represents the P^+ n n^+ diode under the input contact. Included in the DBC diode model are both the recombination under the metal contact and the base input section around the contact under the oxide. Since it was difficult to accurately model an oxide p^+ n n^+ diode with the PN code the region under oxide was included by assuming a saturaton current density under oxide to be 0.1 times the saturation current density under metal. This estimate is based on the work of Berger[9] who used special test structures to measure these current densities. The area of the oxide covered input region is scaled by 0.1 and added to the contact area to determine the saturation current of DBC. The parasitic diodes D2, 3 and 4 are also scaled in area by 0.1 since they are all oxide covered. A parasitic diode was not included under the injector since the injector is grounded to determine fanout. The transistors Q1-Q4 are represented by the GP model for the inverted npn transistor and QI is represented by the GP model for the lateral pnp transistor. The GP bipolar transistor model reproduces the gain versus collector current curve with semi-empirical expressions for I_C and I_B versus V_{BE}. A graph of I_C and I_B versus V_{BE} is used to determine the maximum gain, BF, the collector knee current, IK, the collector saturation current, IS, the ratio of I_B to I_C at $V_{BE} = 0$, C2, and the reciprocal slope of the I_B curve at low currents, NE. These parameters are illustrated in Figure 6 which also shows a comparison between PN code calculated characteristics and the SPICE simulation for the standard npn transistor before irradiation. The low current gain is simulated very well with SPICE up to the maximum gain. However, at currents above the knee current, IK, the collector current has a reciprocal slope of 2 and the base current a slope of 1. Therefore at high currents the gain rolloff is fixed in SPICE. This did not present a major problem

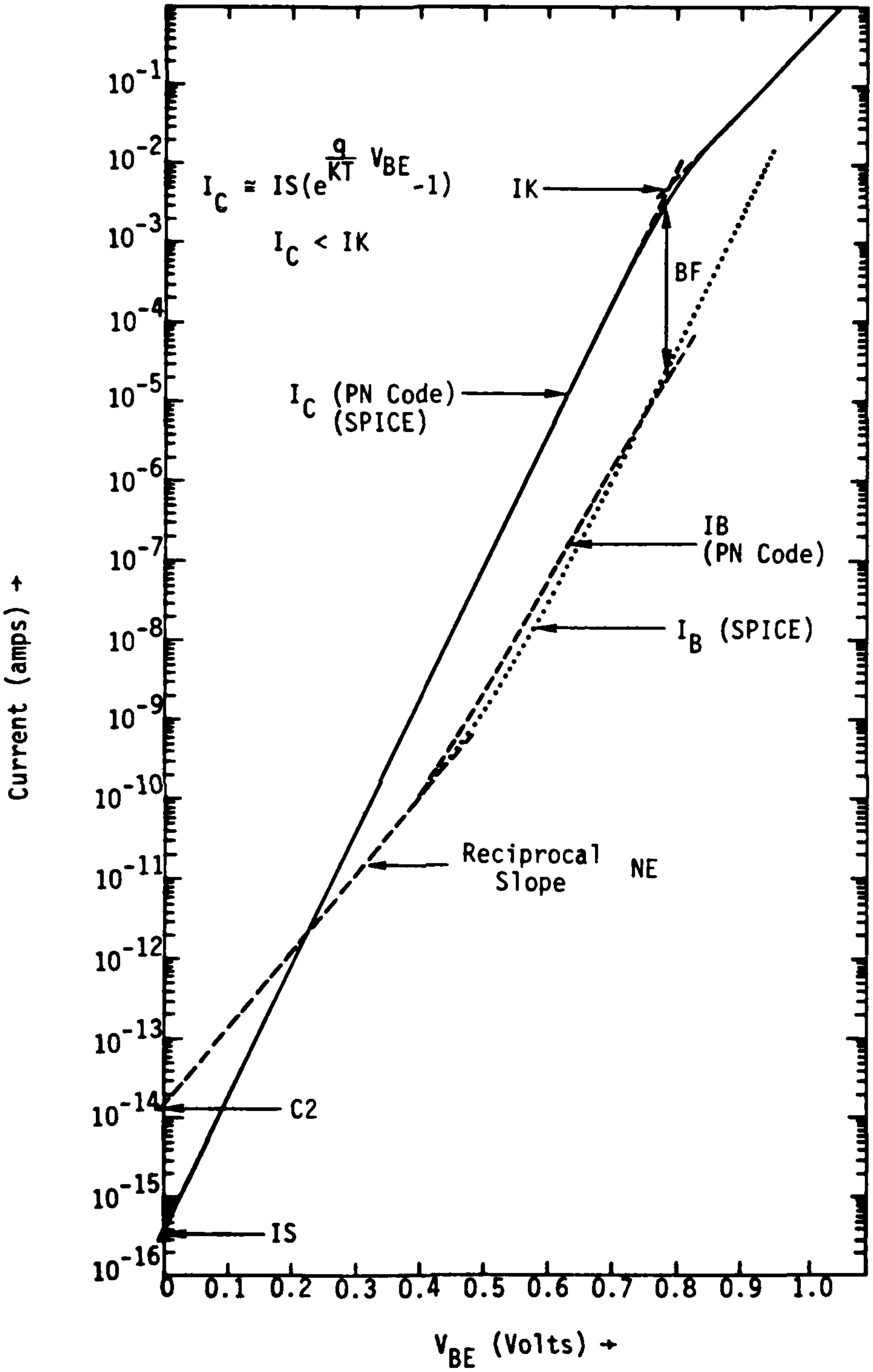

Figure 6. Comparison of PN code calculations and SPICE simulation for standard npn transistor showing GP model parameters.

for the present modeling effort since the region of interest for I^2L operation is at or below the current where maximum gain occurs. However, for modeling photocurrent induced upset due to current overdrive, a more accurate high injection transistor model would be in order.

PREDICTION OF NEUTRON DEGRADED PERFORMANCE

The prediction of fanout versus output current after neutron irradiation is a simple extension of the previously described techniques. In bipolar devices the predominant effect of neutrons is a reduction in carrier lifetime according to the relation

$$\frac{1}{\tau_\phi} - \frac{1}{\tau_o} = \frac{\phi}{K_{n,p}}$$

where τ_ϕ is the lifetime after a neutron fluence ϕ, τ_o the initial lifetimeand $K_{n,p}$ the minority lifetime damage coefficients for n type and p type silicon. In this study the effect of neutrons was determined for each profile by rerunning the code with calculated values of degraded lifetime. The values of K_n and K_p used to calculate the degraded lifetimes were 2.5×10^5 and 5×10^5 sec/cm^2 respectively.

PROCESS VARIATIONS FOR NEUTRON HARDENING

As suggested in previous studies[10], one of the major means of improving the neutron failure level of I^2L logic arrays is to increase the initial fanout per output. The logic array will fail when the fanout per output degrades to the maximum circuit design fanout (number of inputs that an output must sink). In the commercial designs for the I^2L technology used in this study the maximum circuit design fanout is two. This can be reduced to one in order to increase neutron tolerance by circuit design. To further increase neutron hardness by process design, several processing

variations were investigated which would increase the initial fanout margin. The variations that were considered were restricted to a) changes that would not severely degrade switching speed, and b) changes that would not substantially increase processing complexity. With these restrictions the variables considered were p^- base implant concentration, epitaxial thickness and resistivity and pnp transistor base width. Each of these variations resulted in minor modifications to the standard commercial doping density profiles for the various inverter cell components. Table 1 is a list of the variations considered and the components affected in the modeling technique.

TABLE 1

	Process Variation	Components Affected
1.	Reduced p^- implant (0.75, 0.5 and 0.25 times standard)	npn transistor only
2.	Thinner epitaxial layer (n^+ substrate up against P^+)	npn transistor and parasitic diode
3.	Lower resistivity epitaxial (0.5 times standard)	all three
4.	Base Width of pnp (1.5, 0.5 times standard	pnp transistor only
5.	Combined process variation (0.5 times standard p^- implant and thin epitaxial)	npn transistor and parasitic diode

The reduced base implant concentration is expected to yield higher up gains for the npn transistor. The thinner epitaxial layer should also improve the npn gain by increasing emitter efficiency. Both the epitaxial resistivity and the pnp base width will affect the gain and saturation current of the pnp injector. A lower saturation current for the pnp will result in less current back injected into the pnp base and hence more base drive for the npn.

PREIRRADIATION CHARACTERISTICS

The results of the model predictions for preirradiation fanout per collector versus output current are given in Figure 7. The current range of 1 μA to 100 mA encompasses the range of operation for most I^2L applications. In order to illustrate the high current debiasing effect of the extrinsic base resistance, results are shown for the collector nearest to and farthest from the base contact for the standard process. Compared to the standard process, the highest fanouts were predicted for the combined process variation. The reduction in p^- implant concentration resulted in increasing fanout as the concentration was reduced. The thinner epitaxial layer variation resulted in slightly higher fanout with substantial improvement at higher currents. A reduction in the epitaxial resistivity by a factor of two resulted in peak fanouts comparable to the 0.5 p^- implant but more rapid falloff at high and low currents. The variation in pnp base width indicated that increasing the base width would improve fanout while reducing it would decrease fanout.

The results of the SPICE simulations indicated that the primary variables in achieving high fanout are the saturation currents of the pnp (I_{SP}) and npn transistors (I_{SN}). Optimization of fanout is obtained with a high ratio of I_{SN} to I_{SP}. The intrinsic pnp and npn current gains are of primary importance only when the ratio of I_{SN} to I_{SP} is on the order of 10 or greater. The saturation current is proportional to cross-sectional area and diffusion constant and inversely proportional to base width and doping density. Of these variables the ones most affected by the two dimensional aspects of the I^2L inverter cell are the effective cross sectional areas of the npn and pnp transistors and the affective base width of the pnp transistors. For the npn transistor the cross sectional area was assumed to be the area of the n epitaxial above the p^- base implant. For the pnp transistor the area was taken to be the length of the p^+ injector diffusion times the diffusion depth. The base of the pnp was

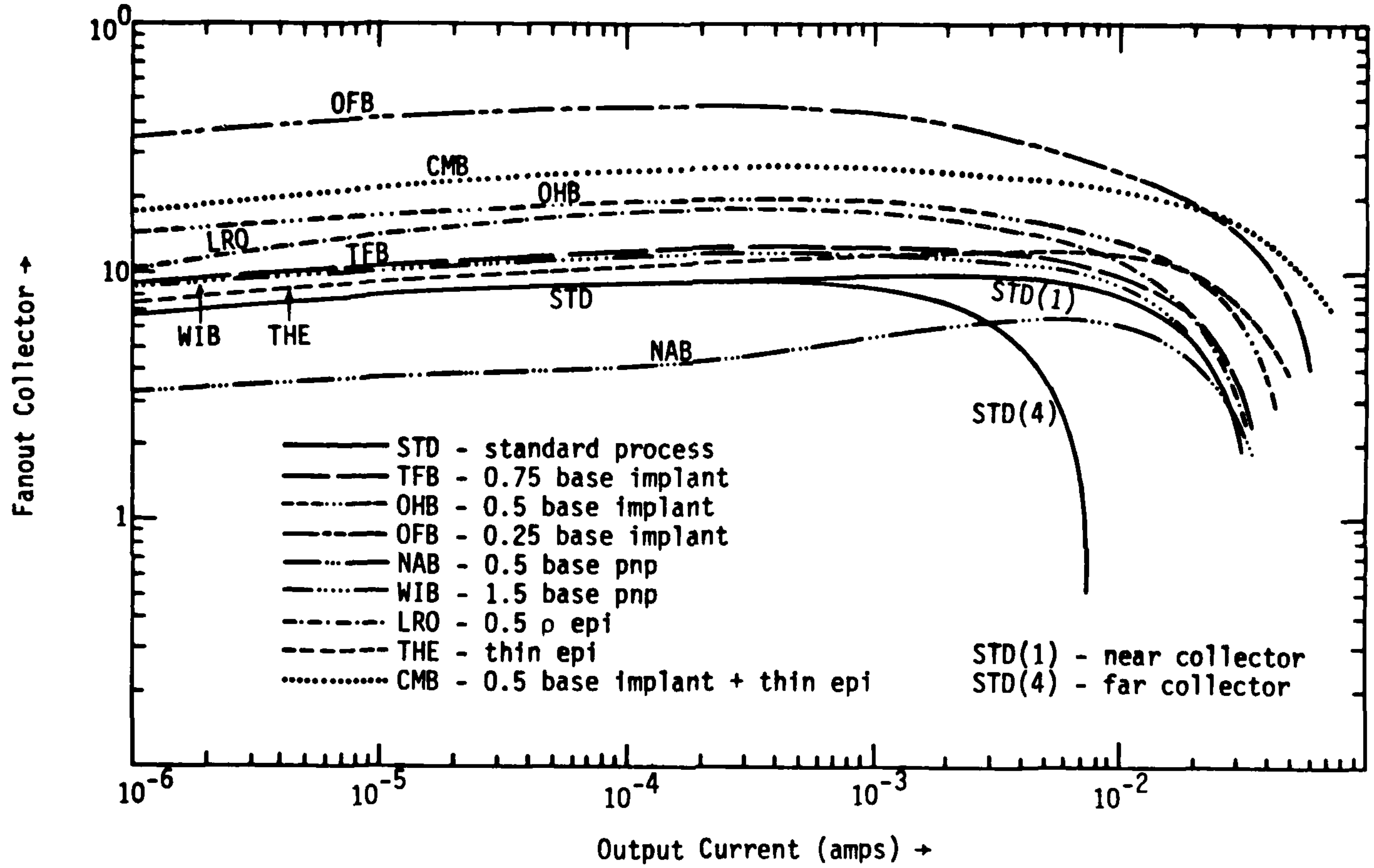

Figure 7. Predicted preirradiation fanout per collector versus output current for standard process and process variations.

determined at a point halfway between the surface and the bottom of the p^+ diffusion. Since there is an uncertainty in the effective values of these parameters for current collection, the ratio of I_{SN} to I_{SP} was adjusted to give fanouts for the standard process which correlated with experimental data taken on test cells by NWSC Crane. In order to fit the data on the standard process, the I_{SN} to I_{SP} ratio was increased by a factor of 2.5. This factor was used consistantly for all process variations both with and without neutron degradation. Such a factor is not unreasonable since the "effective" npn collector area is probably much larger than the actual area due to injection of carriers across the entire npn emitter base area. The ratio of total emitter-base area to total collector area is 2.8.

The improvement in initial fanouts for the reduced p^- implant was due both to an increase of npn gain and I_{SN}. For the thinner epitaxial device, the increase in fanout was due solely to an increase in npn gain since I_{SN} did not increase. The lower resistivity epitaxial resulted in a much smaller I_{SP} with essentially no change in the npn characteristics. The higher fanouts for the wider base pnp were a result of lower I_{SP} and the lower fanout of the narrow base pnp was due to a higher I_{SP}. The combined process benefited both from the increase in I_{SN} from the lower base implant and the increase in gain from both the lower implant and thinner epitaxial.

The only process variations which were available for comparison to predicted results were the 0.5 x standard p^- implant, the thinner epitaxial and the combination of the two. As mentioned previously the ratio I_{SN}/I_{SP} was adjusted to fit the experimental data for the standard process. A comparison between predicted and experimental fanout for the standard process and the process variations is given in Figure 8 for the collector nearest the base contact. The experimental data was taken on a two output inverter cell test structure which also included a metal gate over the pnp base.

The experimental devices used for this study were included on chips that contained a large gate array. Processing difficulties were encountered during fabrication of these devices and consequently the yield on gate arrays was minimal. Although many of the test structures were functional, the devices tested by NWSC Crane showed a wide variation in pre-irradiation response. The data shown in Figure 8 is an average of two inverter cells preselected from a sample of 10 for optimimum fanout. Although it was intended that the thin epitaxial devices have the n^+ substrate up against the p^- implant, angle lap measurements indicated that this was not achieved. Therefore, while the amount of n epitaxial under the p^- base was reduced in the thin epitaxial devices, it was not eliminated. Because of the difficulties encountered with the processing of the test devices, a detailed comparison to predictions is not warranted. However, a general comparison does indicate that thinning the epitaxial layer results in minimal improvement of fanout and reducing the base implant concentration yields substantial improvement in fanout as predicted. Combining the process variations gave the best results. The high current roll off of fanout in the experimental devices occurred at much lower values of output current than predicted. This can be attributed to the use of a one dimensional model for the intrinsic transistors which does not account for lateral debiasing along the emitter-base junction, especially in the npn transistor.

POST IRRADIATION CHARACTERISTICS

Each of the process variations were modeled for neutron degradation of fanout per collector versus output current at 10^{13} n/cm^2. A comparison of these predictions to the experimental results on the standard, one half base implant, thin epitaxial layer and combined process is shown in Figure 9. The predicted results for the standard process agree reasonably well except at high currents. The predictions for the 0.5 base implant concentration agree at peak fanout, however the predicted results at low currents

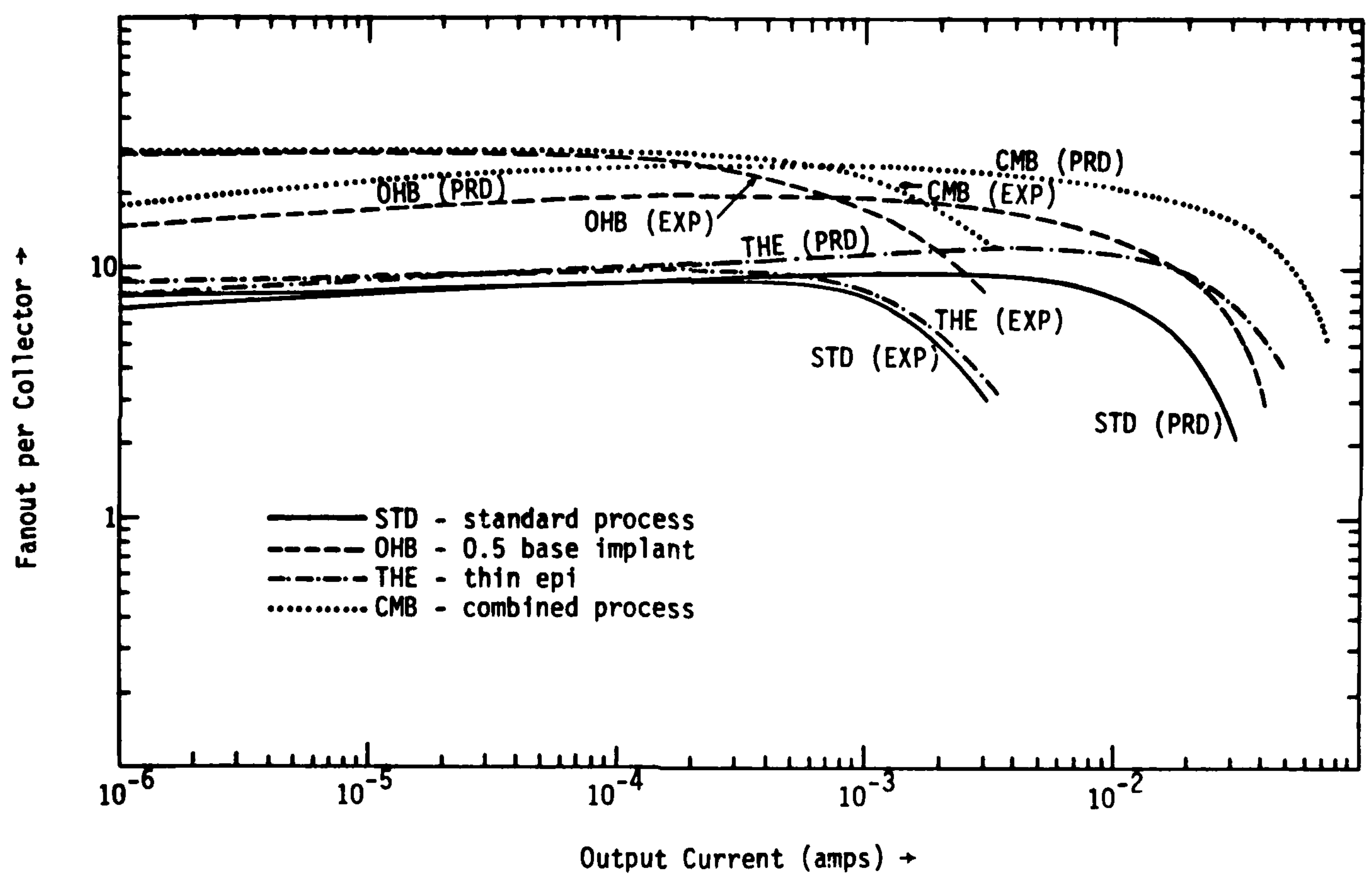

Figure 8. Comparison of predicted and experimental fanout per collector versus output current for standard process and process variations.

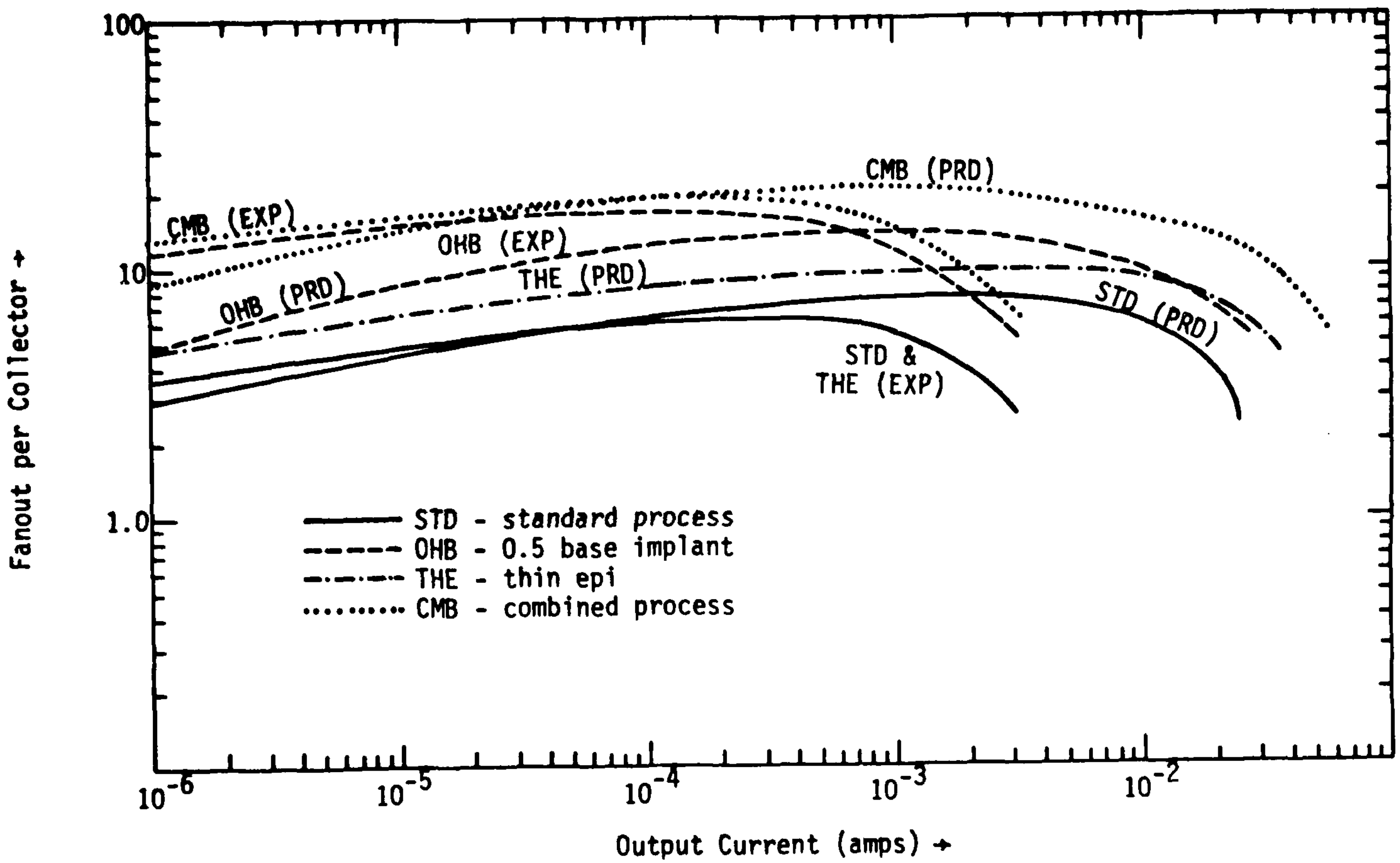

Figure 9. Comparison of predicted and experimental fanout per collector versus output current for standard process and variations of the standard process after a neutron fluence.

show a much greater roll off than observed experimentally. For the thin epi process the predicted degradation is much less than that observed experimentally. This is probably due to the fact that the experimental devices did not have the n^+ substrate up against the p^- base as it was in the modeled device. Therefore the experimental thin epitaxial layer device would be expected to perform only slightly different from the standard device. The predicted results for the combined process agreed reasonably well with experimental measurements, again with the exception of high current roll off. The results of the predictions are best compared to the experimental results through equation

$$\frac{1}{FO(\phi)} - \frac{1}{FO(0)} = K_{FO}\phi$$

where $FO(\phi)$ is the degraded fanout per collector, $FO(0)$ is the initial fanout per collector, K_{FO} the fanout damage coefficient and ϕ the neutron fluence in n/cm^2. The damage coefficient, which is a measure of the rate of degradation, is a good measure of relative hardness. In Table 2 the initial and degraded fanouts are given at 100 μA collector current along with the damage coefficient both for the predicted and experimental results.

A comparison of the damage coefficients for the process variations as compared to the standard process indicate the following:

a. A reduction in the p^- implant concentration not only increases initial fanout but results in a reduced damage coefficient. These results are supported by the experimental data.

b. While the thinner epitaxial layer results in only a minor increase in fanout, the predicted damage coefficient is half that of the standard process. This result was not verified experimentally. However, as previously pointed out, the experimental device did not have the epi under the p^- base eliminated.

c. The lower epitaxial resistivity gave higher initial fanout but did not result in a substantial reduction in damage.

d. Variations in pnp base width resulted in moderate changes in fanout not very minor changes in damage coefficient. The results indicated that higher fanouts could be achieved with a wider base.

e. The best results are obtained using a combination of thinner epi and reduced p^- implant concentration. The predicted results correlated very well with experimental data. Since the damage coefficient for the combined process was less than for the 0.5 base implant along, it is clear that the thin epi does improve hardness as predicted.

Table 2. Comparison of Predicted and Experimental Damage Coefficients.

Predicted Response at 100 μA Output Current

Symbol		(FO(0)	FO(μ)	K_{FO}(x 10^{-15}) (cm)
STD	Standard commercial	8.85	6.14	4.99
TFB	0.75 x STD p- implant	11.9	7.94	4.19
OHB	0.5 x STD p- implant	19.1	12.1	3.03
OFB	0.25 x STD p- implant	45.6	23.3	2.10
THE	Thin Epitaxial	10.2	8.23	2.35
CMB	0.5 x STD p- implant + thin epi	25.4	19.0	1.33
LRO	0.5 x STD epi ρ	16.8	9.93	4.12
WIB	1.5 x STD pnp base width	11.4	7.37	4.80
NAB	0.5 x STD pnp base width	4.1	3.34	5.55
	Experimental Response at 100 μA Collector Current			
STD	Standard	8.9	6.05	5.29
OHB	0.5 x STD p- implant	27.2	17.0	2.21
THE	Thin epitaxial	9.8	6.05	6.32
CMB	0.5 x STD p- + thin epi	28.6	19.3	1.68

Using the predicted damage coefficients for the various process modifications, fluence of failure calculations were made for circuit design fanouts of 2 and 1. For the I^2L technology used in this study a design fanout of 2 would correspond to a commercial design and a fanout of 1 to a hard design. Table 3 is a list of the calculated fluence of failure as determined from the predicted K_{FO}s.

TABLE 3. Predicted Fluence of Failure for Process Variations.

Process	ϕ_F* Design FO = 2 ($\times 10^{14}$ n/cm^2)	ϕ_F* Design FO = 1 ($\times 10^{14}$ n/cm^2)	$\frac{\phi_F(FO) = 1)}{\phi_F(FO = 2) (STD)}$
STD	0.775	1.78	2.30
TFB	0.992	2.19	2.83
OHB	1.48	3.13	4.04
OFB	2.28	4.66	6.01
THE	1.71	3.84	4.95
CMB	3.46	7.22	9.32
LRO	1.07	2.28	2.94
WIB	0.859	1.90	2.45
NAB	0.461	1.36	1.75

*Based on damage coefficient at 100 μA collector current.

The predicted failure levels given in Table 3 are based on nominal predicted response using damage coefficients calculated at 100 μA collector current. Since the damage coefficient is a strong function of current, the failure level would be lower at lower operating currents. The last column in Table 3 is the ratio of failure fluence for a radiation hard design to the failure fluence of the standard process using a commercial design. Thus it is a measure of the predicted increase of failure level expected when the process variation is combined with a radiation hard design. The change in design alone would yield a factor of 2.3 increase in failure level. The best results would be for the combined process which would give a factor of 9.3 increase over the commercial part.

The process variations were chosen to have minimal impact on the commercial process. However, some difficulties may arise in implementing

necessary to maintain sufficient breakdown on the outputs. The thinner epitaxial is harder to control and may result in wider variation in inverter characteristics due to epitaxial thickness variations. Also the thinner epi will cause a higher emitter-base capacitance on the npn transistors which would reduce the switching speed. The lower resistivity epi will also increase the emmitter-base capacitance and hence reduce speed.

SUMMARY

A modeling technique has been developed and applied to I^2L inverters to predict the neutron degradation of fanout versus output current for a standard commercial I^2L process and variations of the process to increase neutron hardness. The technique is equally applicable to arbitrary geometries and processes. Good agreement was obtained in comparing predicted response to experimental data on test devices fabricated with the standard process and three variations of the process. The results of the predictions indicate that for the process variations considered, maximum failure fluence is achieved by reducing the p^- base implant concentration and eliminating the n epitaxial region under the npn base. Not all process variations which gave predicted fanouts higher than the standard process resulted in a substantial increase in hardness. Both wider base pnp and the lower ρ epitaxial gave significantly higher initial fanouts with very little improvement in hardness, while the thin epitaxial process predictions yielded only a modest improvement in initial fanout with a substantial increase in hardness.

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4 cy ATTN: TITL

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12 cy ATTN: DD

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BMD Systems Command
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Deputy Chief of Staff for Rsch Dev & Acq
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U.S. Army Armament Rsch Dev & Cmd
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ATTN: DELHD-N-RBH, H. Eisen
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U.S. Army Material & Mechanics Rsch Ctr
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U.S. Army Missile Command
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Naval Weapons Center
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Strategic Systems Project Office
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ATTN: NTYC, Capt Swenson
5 cy ATTN: NTYC

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ATTN: AQM

Headquarters Space Division
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Air Force Systems Command
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Department of the Air Force
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National Bureau of Standards
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Institute for Defense Analyses
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